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1	soi and (fet mosfet nfet pfet nmosfet pmosfet) and spice
2	soi and (fet mosfet nfet pfet nmosfet pmosfet) and spice and (output load) with (resist\$5 capacit\$5)
3	soi and (fet mosfet nfet pfet nmosfet pmosfet) and spice and (output load) with (resist\$5 capacit\$5) and body near3 charg\$4
4	soi and (fet mosfet nfet pfet nmosfet pmosfet) and spice and (output load) with (resist\$5 capacit\$5) and body near3 charg\$4 and @ad<"20021128"
5	soi same (fet mosfet nfet pfet nmosfet pmosfet) and spice and (output load\$4) same (resist\$5 capacit\$5) and body with charg\$4 and @ad<"20021128"
6	soi and (fet mosfet nfet pfet nmosfet pmosfet cmos) and spice and (output load\$4) same (resist\$5 capacit\$5) and body with charg\$4 and @ad<"20021128" and partial\$4 with deplet\$6
7	soi and (fet mosfet nfet pfet nmosfet pmosfet cmos) and (output load\$4) same (resist\$5 capacit\$5) and body with charg\$4 and @ad<"20021128" and partial\$4 with deplet\$6
8	soi and (fet mosfet nfet pfet nmosfet pmosfet cmos) and (output load\$4) same (resist\$5 capacit\$5) and body with charg\$4 and @ad<"20021128" and partial\$4 with deplet\$6 and (transient near2 anal\$7 fluctuat\$5)
9	soi and (fet mosfet nfet pfet nmosfet pmosfet cmos) and (output load\$4) same (resist\$5 capacit\$5) and body with (charg\$4 current)and @ad<"20021128" and partial\$4 with deplet\$6 and (transient near2 anal\$7 fluctuat\$5)
10	x same y same ratio and @ad<"20021128" and partial\$4 with deplet\$6
11	x same y same ratio and @ad<"20021128" and partial\$4 with deplet\$6 and (body same (current charge))
12	pd near2 soi and @ad<"20021128"
13	pd near2 soi and @ad<"20021128" and spice and resistance and capacitance
14	partial same deplet\$5 same silicon same insulat\$5 and @ad<"20021128" and spice and resistance and capacitance
15	partial\$5 same deplet\$5 and soi and @ad<"20021128" and spice and resistance and capacitance
16	partial\$5 same deplet\$5 and soi and @ad<"20021128" and zero same fluctuat\$4 same body and (resistance capacitance)
17	partial\$5 same deplet\$5 and soi and @ad<"20021128" and (resistance capacitance) and estimat\$4 same body same current
18	partial\$5 same deplet\$5 and soi and @ad<"20021128" and (resistance capacitance) and estimat\$4 same body same current and (noise transient) with anal\$7
19	partial\$5 same deplet\$5 and soi and @ad<"20021128" and (resistance capacitance) and estimat\$4 same body same current and (noise transient) and (spice simulat\$5)
20	partial\$5 same deplet\$5 and soi and @ad<"20021128" and (resistance capacitance) and estimat\$4 same body same (charg\$4 current)and (noise transient)
21	partial\$5 same deplet\$5 and soi "716"/\$.ccls. and @ad<"20021128"
22	partial\$5 same deplet\$5 and soi and "716"/\$.ccls. and @ad<"20021128" and body adj2 (current charg\$5) and (signal cycle pulse) with (maxim\$7 increas\$5 elongat\$4 adjust\$6)

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23	partial\$5 same deplet\$5 with silicon with insulator or pd-soi and @ad<"20021128" and body adj2 (current charg\$5) and (signal cycle pulse) with (maxim\$7 increas\$5 elongat\$4 adjust\$6) and (resistance or capacitance) with (load output)
24	(partial\$5 same deplet\$5 with silicon with insulator or pd-soi) and @ad<"20021128" and body adj2 (current charg\$5) and (signal cycle pulse) with (maxim\$7 increas\$5 elongat\$4 adjust\$6) and (resistance or capacitance) with (load output)
25	(partial\$5 same deplet\$5 with silicon with insulator or pd-soi) and @ad<"20021128" and body adj2 (current charg\$5) and (signal cycle pulse) with (maxim\$7 increas\$5 elongat\$4 adjust\$6) and (resistance or capacitance) and (steady adj state) same (partial\$5 same deplet\$5 with silicon with insulator or pd-soi)
26	(spice simulat\$5) and soi and (fet mosfet nfet pfet nmosfet pmosfet cmos) and partial\$4 near4 deplet\$5 and (increas\$4 elongat\$4 expans\$5) same (input signal pulse cycle duration)
27	(spice simulat\$5) and soi and (fet mosfet nfet pfet nmosfet pmosfet cmos) and partial\$4 near4 deplet\$5 and (increas\$4 elongat\$4 expans\$5) same (input signal pulse cycle duration) and steady adj state
28	(spice simulat\$5) and soi and (fet mosfet nfet pfet nmosfet pmosfet cmos) and partial\$4 near4 deplet\$5 and (increas\$4 elongat\$4 expans\$5) same (input output signal pulse cycle duration load) and (fluctuat\$4 transient)
29	(spice simulat\$5) and soi and (fet mosfet nfet pfet nmosfet pmosfet cmos) and partial\$4 near4 deplet\$5 and (increas\$4 elongat\$4 expans\$5 simulat\$4) same (input waveform output signal pulse cycle duration load) and (fluctuat\$4 transient)
30	(spice simulat\$5) and soi and (fet mosfet nfet pfet nmosfet pmosfet cmos) and partial\$4 near4 deplet\$5 and (increas\$4 elongat\$4 expans\$5 simulat\$4) same (input waveform output signal pulse cycle duration load) and (fluctuat\$4 transient) same (body current charg\$5)
31	(spice simulat\$5) and soi and (fet mosfet nfet pfet nmosfet pmosfet cmos) and partial\$4 near4 deplet\$5 and (increas\$4 elongat\$4 expans\$5 simulat\$4) same (input waveform output signal pulse cycle duration load) and (steady adj state)
32	(spice simulat\$5) and soi and (fet mosfet nfet pfet nmosfet pmosfet cmos) and partial\$4 near4 deplet\$5 and (increas\$4 elongat\$4 expans\$5 simulat\$4) same (input waveform output signal pulse cycle duration load) and (resistance capacitance) and (steady adj state)
33	(initial\$4) near3 (value state) and (spice simulat\$5) and soi and (fet mosfet nfet pfet nmosfet pmosfet cmos) and partial\$4 near4 deplet\$5 and (increas\$4 elongat\$4 expans\$5 simulat\$4) same (input waveform output signal pulse cycle duration load) and (resistance capacitance) and (steady adj state)
34	(spice simulat\$5) and soi and (fet mosfet nfet pfet nmosfet pmosfet cmos) and partial\$4 near4 deplet\$5 and (increas\$4 elongat\$4 expans\$5 simulat\$4) same (input waveform output signal pulse cycle duration load) and (steady adj state) and (fluctuat\$5 transient\$4 deviation) same (charg\$4 current\$4)